REMARKS

Claims 1-27 were examined in the present application and were rejected. Claims 1, 6, 15 and 23 have been amended for clarification purposes and to correct typographical errors only, and new claims 28 through 33 are added. No new matter has been added and claims 1-33 remain pending in the application.

Claim amendments are entered herein as follows. Claim 1 is amended to remove the "using a differential amplifier" example and thereby more properly recite a method embodiment (that might utilize a differential amplifier or other suitable apparatus/system related elements, as discussed in the specification), as originally claimed. Claims 6 and 15 are amended to replace the "synchronous" reference and signal terminology with terminology more clearly expressing that the oscillating reference and incoming signal of the recited embodiment merely should be "received substantially synchronously" in the recited embodiment (e.g. see FIGS. 3b and 10). Finally, while Applicant believes that the coupling of one of two comparators necessarily leaves an "other" uncoupled comparator, the amended language of claim 23 more directly expresses that the recited embodiment includes circuitry for de-coupling a coupled comparator and for coupling an uncoupled comparator.

Support for new claims 28-33 includes the following. New claims 28 and 30, which recite embodiments in which the oscillating references of system claim 1 and method claim 11 respectively can comprise a "ramp signal", are supported at least by the specification at page 17, line 6. New claims 29 and 31, which recite that the oscillating references of system claim 1 and method claim 11 respectively can be "discontinuously varying", are supported at least by FIG. 10. Finally, new claims 32 and 33, which recite that the "first controller" and "second controller" of claims 11 and 19 respectively can include an "exclusive-OR (XOR) logic gate", are supported at least by FIG. 4 and page 12, line 15 through page 13, line 2 of the specification.

It is to be understood that the above remarks regarding the presently pending claims are provided merely to clarify that the present claims are supported in the specification and the amendments being made herein do not add new matter. The present

claims are not limited to the specific embodiments cited above for the intended limited purpose.

Telephone Interview

Applicant thanks the Examiner for the telephone interview of January 7, 2001 between the Examiner and Applicant's representative, and the Examiner's assistance in connection therewith. The following summarizes the substance of the telephone interview.

The Examiner, however, after agreeing that the following place the application in a condition for allowance, called Applicant's Attorney suggesting that some further objection/rejection might yet exist. Unfortunately, Applicant's request for elaboration was met with a promise by the Examiner to provide a written explanation which writing remains forthcoming. Applicant must presume by the Examiner's silence that the application is INDEED placed in a condition for allowance by this amendment. Conversely, requiring the Applicant to pay still further unnecessary extension fees while waiting for such explanation would certainly be unfair, and uncharacteristic of the Examiner's assistance thus far in keeping with the stated USPTO goal of moving prosecution forward.

Claim Rejections - 35 U.S.C. § 112

On page 2 of the Office Action, the Examiner rejected claims 1-19 and 23-27 under 35 U.S.C. § 112, second paragraph, as being indefinite and requiring correction or clarification. Applicant respectfully traverses.

Regarding claims 1, 11 and 19, the Examiner asserted that it is unclear what the "known previous logical state" is and how the differential amplifier can detect a transition in the incoming signal relative to the known previous logic state and how this limitation is read on the preferred embodiments or seen on the drawings.

However, having obtained an oscillating reference and received an incoming signal, a transition in the incoming signal relative to the known previous logic state can clearly be detected in accordance with embodiments of the invention. Examples of such

embodiments are further provided throughout the specification and drawings, among other potential embodiments.

For example, the embodiment of page 14, lines 5-13 discusses "If the transition has occurred in the single-ended signal SNx, the output signal SN has the new level opposite to its previous signal level. Since both SSVTR (or /SSVTR) and single-ended signals have transitioned, the same comparator 410 is still coupled to the signal output terminal. If the single-ended signals SNx have not transitioned, then the signal output SN does not change, the comparator 410 coupled at the start of the transition is de-coupled from the output after the SSVTR and /SSVTR receiver has amplified their new binary state (VT & /VT), and the other comparator 410 which has opposite /SSVTR (or SSVTR) is coupled to provide the signal output. The old output level is thereby restored."

The Examiner correctly pointed out during the above telephone interview that determining whether the particular "old" signal level is "high" or "low" is not needed; rather, only change or lack of change with respect to the prior signal level should be detected. However, as the Examiner agreed, the current claim language recites such intent more clearly than other alternatives that might otherwise be used.

Therefore, withdrawal of the rejection is respectfully requested.

Regarding claims 2, 4-5 and 13-14, the Examiner asserted on Page 3 of the Office Action that "it is unclear how the result can drive an output signal." Applicant respectfully traverses.

During the above telephone interview, however, the Examiner admitted that it is indeed clear how the result can drive an output signal. (See, for example, the embodiments of FIG. 4 and the specification at page 12, line 4 through page 15, line 12.)

Therefore, withdrawal of the rejection is respectfully requested.

Regarding claims 11 and 19, the Examiner asserted on Page 3 of the Office Action that "it is unclear how the controller can couple[ed] the first result to the output

terminal and how this limitation is read on the preferred embodiment or seen on the drawings." Applicant respectfully traverses.

Claim 11 recites:

> "11. A system for detecting a transition in an incoming signal from a known previous logical state, comprising:
>
> first and second input terminals for receiving, respectively, an oscillating reference and an incoming signal;
>
> an output terminal providing an output signal logically equal to the previous logical state;
>
> a first comparator coupled to the first and second input terminals for comparing the reference and the incoming signal to generate a first result; and
>
> a first controller coupled to the first comparator for coupling the first result to the output terminal based on the previous logical state."

And claim 19 recites:

> "19. (Once Amended) The system of claim 11, further comprising:
>
> a third input terminal for receiving an oscillating reference complement;
>
> a second comparator coupled to the second and third input terminals for comparing the complement and the incoming signal to generate a second result; and
>
> a second controller coupled to the second comparator for coupling the second comparator to the output terminal based on the previous logical state."

Clearly, the "first controller coupled to the first comparator" of claim 11 is capable of "coupling the first result to the output terminal based on the previous logical state" and the "second controller coupled to the second comparator" is capable of "coupling the second comparator to the output terminal based on the previous logical state" in accordance with embodiments of the invention. Examples of such embodiments

are further provided throughout the specification and drawings, among other potential embodiments.

For example, the embodiment of page 12, line 11 through page 13, line 17 discusses, "SSVTR is initially set to VOL and /SSVTR and SNx are initially set to VOH. SN is initially set to a full rail high output voltage. Accordingly, the comparator 410a amplifies high voltage SNx minus low voltage SSVTR, thereby providing a high output signal. The comparator 410b amplifies high voltage SNx minus high voltage /SSVTR, providing a noise-amplified unknown output signal. Switch 415 selection is controlled by exclusive-OR (XOR) logic gates 425. More particularly, XOR gate 425a compares a full rail SSVTR amplified signal (VT) against output signal SN, and generates a control signal for controlling switch 415a. XOR gate 425b compares full rail /SSVTR (/VT) against output signal SN, and generates a control signal for controlling switch 415b. In this initial state, only SSVTR and accordingly VT are low, thereby causing XOR 425a to drive switch 415a closed. Accordingly, the comparator 410a output (high) reaches output terminal 420. XOR 425 drives switch 415b open, thereby preventing the entry of the unwanted output signal from comparator 410b. Receiver 405 is stable.

Following the example illustrated in FIG. 3B, the single-ended signal SNx transitions to a low voltage. As always, SSVTR and /SSVTR transition opposite to one another. Accordingly, as soon as SSVTR and /SSVTR achieve a predetermined difference (preferably 250mV) therebetween, VT and /VT transition. Similarly, as soon as SSVTR and SNx transition to a predetermined difference (preferably 250mV) therebetween, the output of comparator 410a also transitions (to a low output voltage). It will be appreciated that the path from external signal SNx to the generation of output signal SN and the path for full rail signal VT and /VT generation path each include one comparator 410 or 435 and two inverters 430 or 440. Thus, each XOR 425 will receive new input signals based on the speed of the comparison by the comparators 410 and 435. In this example, as evident by the example timing diagram of FIG. 3B, SSVTR and /SSVTR will achieve a predetermined difference at the same time that SSVTR and SNx achieve the same predetermined difference. Accordingly, the XOR 425a will continue to receive differential inputs, thereby maintaining the same switch 415a closed and enabling the low output voltage of comparator 410a to pass to output terminal 420."

In this example, the controllers (including XORs 425a-b) are clearly capable of the coupling recited in claims 11 and 19. These more specific examples are also more specifically claimed in the embodiments recited by new claims 32 and 33 respectively.

Therefore, withdrawal of the rejection is respectfully requested.

Regarding claims 6 and 15, the Examiner asserted on page 3 of the Office Action that it is unclear how the reference can be "synchronous" with the "incoming signal". Applicants respectfully traverse.

Applicant respectfully submits and the Examiner admitted during the above telephone interview that the reference can be "synchronous" with the "incoming signal". However, Applicant also agreed with the Examiner that the reference need not be synchronous with the incoming signal and should only be "received substantially synchronously" with the incoming signal, and claims 6 and 15 are amended accordingly herein. (Substantially, in this case, includes skew or other factors that might cause somewhat non-synchronous results to which embodiments of the invention can nevertheless be directed, e.g. see FIG. 10).

Therefore, withdrawal of the rejection is respectfully requested.

Regarding claims 23, the Examiner asserted on page 3 of the Office Action that it is unclear how the recitations "the comparator" and "the other comparator" lack antecedent basis. Applicants respectfully traverse.

Unamended claim 23 recites:

> "23. (Once Amended) A receiver comprising:
>
> a first comparator for comparing an oscillating reference and a new signal;
>
> a second comparator for comparing a complement of the oscillating reference and the new signal;
>
> an output terminal coupled to one of the first and second comparators;

circuitry for maintaining the comparator that is coupled to the output terminal coupled to the output terminal when the new signal transitions; and

circuitry for coupling the other comparator to the output terminal and de-coupling the coupled comparator from the output terminal when the new signal does not transition."

While the word "the" and "the other" are recited, an antecedent basis is provided for at least line 6 ("the comparator") by "an output terminal coupled to *one of the first and second comparators*" (emphasis added). It is also submitted that the same phrase also provides antecedent basis for the "other" comparator. As was noted above, however, claim 23 has nevertheless been amended to more directly establish antecedent basis and greater clarity. Difficulty in further amending claim 23 also arises in that "the oscillating reference" and its "complement" should not be associated with particular reference components, such as a non-barred reference and a barred compliment; rather, such references are necessarily each compliments of the other. Thus, the unamended or amended claims most clearly express the recited embodiment.

Therefore, withdrawal of the rejection is respectfully requested.

Double Patenting

The Examiner further rejected claims 1-27 with reference to U.S. Patent No. 6,160,423 under the judicially created doctrine of obviousness type double-patenting. Applicant respectfully traverses.

The Examiner agreed during the above-noted telephone interview that the double-patenting rejection should have been and is now entered as merely provisional, pending allowance, such that no further response is appropriate at this time.

Therefore, withdrawal of the current rejection is respectfully requested.

Claim Rejections - 35 U.S.C. § 102(e) over Dumas

The Examiner further, on page 3 of the Office Action, rejected claims 1 and 6-8 under 35 U.S.C. § 102(e) over U.S. Patent 6,122,331 to Dumas ("Dumas"), asserting only that Figure 6 of Dumas discloses a detection circuit comprising an amplifier. Applicant respectfully traverses.

Dumas at least does not teach or suggest "obtaining an oscillating reference", as in the embodiment recited by claim 1, which the Examiner admitted during the above telephone interview. Nevertheless, the Examiner also admitted that the amendment herein to claim 1 deletes the previously recited "differential amplifier" which formed the basis for the rejection, thereby rendering the rejection moot. Moreover, claims 6-8 are dependent claims depending from claim 1 and are patentable over Dumas for at least the same reasons that claim 1 is patentable over Dumas.

Therefore, withdrawal of the rejection is respectfully requested.

Conclusion

For at least the above reasons, claims 1-33 are in condition for allowance. If the next communication is other than a Notice Of Allowance, the Examiner is invited to telephone the undersigned attorney at (650) 843-8796.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version With Markings To Show Changes Made."**

If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 05-0150.

Respectfully Submitted,

Dated: 3/11/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

The paragraph beginning at page 10 line 3 has been amended as follows:

-- As shown in FIG. 3A, the SSVTR and /SSVTR signals toggle every time ~~the~~ valid signals are driven by the master 205. It will be appreciated that slave 210 may include multiple receivers (405, FIG. 4), wherein each receiver 405 includes two comparators, one for comparing the signal against SSVTR and the other for comparing the signal against /SSVTR. A present signal binary value determines which comparator is coupled to the output terminal 420, optionally by using exclusive-OR logic with SSVTR and /SSVTR. Until SSVTR and /SSVTR have changed their binary value, the enabled comparator in the receiver 405 detects whether change in signal binary value occurred. --

The paragraph beginning at page 12 line 4 has been amended as follows:

-- FIG. 4 (4-1 and 4-2) is a high level schematic illustrating a single-ended signal slave 210, having a receiver 405 for each signal line 215. Each signal receiver 405 has two comparators 410, one comparator 410a for comparing an incoming single-ended signal "SNx" to SSVTR and the other comparator 410b for comparing SNx to /SSVTR. Both of the comparators 410 have output terminals selectively coupled via switches 415 to an output terminal 420. It will be appreciated that the output signal (SN) to the output terminal 420 is preferably a full rail signal (0V to 2.5V). --

The paragraph beginning at page 15 line 13 has been amended as follows:

-- FIG. 5 (5-1 and 5-2) is a flowchart a method 500 of communicating signals from a master 205 across a transmission line 215 to a receiver 405. Method 500 begins with the master 205 in step 505 setting SSVTR to VOL and all single-ended signals (/SSVTR and SNx) to VOH, and in step 510 setting all single-ended receiver outputs (SN)

to a full rail high. The receiver 405 in step 515 couples the comparator 410a, which compares SSVTR against each single-ended signal SNx, to the output terminal 420 of the receiver 405. The receiver 405 in step 517 lets all signals on the transmission lines settle down. Steps 505-517 are referred to as system initialization. --

The paragraph beginning at page 17 line 6 has been amended as follows:

-- For a uniformly transitioning ramp-like signal, the preferred slew rate of signals is four times the sum of two inverter delays and an exclusive-OR delay in a given technology. In 0.25μ CMOS technology with an operating voltage of 2.5V, the inverter delay is 50 picoseconds and the exclusive-OR delay is approximately 120 picoseconds. Thus, the preferred slew rate is approximately 880 picoseconds. For signals transmitted above the rate of 600MHz, the signal slew rate is preferably less than 110% of the signal rate. The preferred slew rate for exponential signals is slightly faster if the signal reaches 75% of its final value earlier than ¾ of the transition time. The differential signals preferably cross half way through the voltage transition. At around ¾ of the way through the voltage transition, the signals have a difference of about 250mv which can be converted quickly to a large swing signal. To avoid noise amplification and to prevent signal coupling to the receiver output upon receipt non-transitioning single-ended signals, the transition time between 75% and the final signal value is preferably higher than the sum of two inverter delays and the exclusive-OR delay. It will be appreciated that the slew rate can go as fast as it takes amplified noise to reach the output of the comparator 410 whose output is coupled to the output terminal 420. That is, upon receiving a non-transitioning signal, the switches 415 switch state before the comparator output changes state based on noise amplification. The output of the currently coupled comparator 410 approaches an undetermined (noise amplified) state. The switches 415 must switch states before the undetermined output becomes available. It will be further appreciated that device mismatches, manufacturing tolerances and signal reflection will ~~effect~~ affect the speed at which the output of the comparator 410 reaches the undetermined state. As the technology improves, gate delays, faster slew rates and faster signal rates will be achievable. --

The paragraph beginning at page 22 line 12 has been amended as follows:

-- FIGs. 8A and 8B are schematic diagrams illustrating circuit details corresponding to comparators 435 of FIG. 4. Each comparator 435 includes a differential amplifier 802 (FIG. 8A) or 852 (FIG. 8B) similar to the differential amplifier 702 of FIGs. 7A and multiple inverters 804 (FIG. 8A) or 854 (FIG. 8B) in series. The full rail output signals of the comparators 802 and 852 (VT1, VT2, VT3, /VT1, /VT2 & /VT3) are transmitted to all the single-ended receivers' XORs 425 (FIG. 4). Selection of VT1, VT2 or VT3 is determined based on testing for signal speed substantially equal to that of the receiver 405 output signal SN generation path. --

The paragraph beginning at page 22 line 20 has been amended as follows:

-- FIG. 9 (9-1 and 9-2) is a schematic diagram illustrating receivers 405 with individually adjustable delays to eliminate skew during transmission and to convert small swing to large swing by comparators 410. To tune the operating frequency or voltage swing for optimum performance, each receiver 405 has a register 905 for storing data to enable delivery of one of the three VT1 & /VT1, VT2 & /VT2 or VT3 & /VT3 to the XOR 425 (FIG. 4). --

The paragraph beginning at page 22 line 20 has been amended as follows:

-- By using devices with very low power dissipation and close physical packing, the bus can be made as short as possible, which in turn allows for short propagation times and high data rates. As shown in FIG. 2B, the resistor-terminated controlled-impedance transmission lines can operate at signal rates of 1Ghz (1ns per cycle). The characteristics of the transmission lines are strongly affected by the loading caused by integrated circuits like DRAMs mounted on the bus. These integrated circuits add lumped capacitance to the lines, which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the bus impedance is likely to be on the order of 25

ohms and the propagation velocity of 7.5cm/ns. Care should be taken not to drive the bus from two devices at the same time. So for buses less than about 12cm, one dead cycle (e.g., 2ns) is needed to settle the bus for switching from one driver to another driver. For longer buses, more than one cycle may be needed for the signals to settle down before a new transmitter can drive the signal. Unlike RAMBUS, the length of the bus does reduce operating frequency in burst mode from the same device. --

In The Claims:

Please amend *EXISTING* claims 1, 6, 15 and 23 as follows: (Note that, for the Examiner's convenience, claims remaining in the present application that are not being amended are reproduced in italics and claims that are being amended herein are preceded by a double asterisk.)

** 1. (Twice Amended) A method of detecting a transition in an incoming signal from a known previous logical state, comprising:

obtaining an oscillating reference;

receiving an incoming signal; and

comparing the oscillating reference against the incoming signal ~~using a differential amplifier~~ to detect a transition in the incoming signal relative to the known previous logical state.

2. The method of claim 1, wherein comparing includes generating a first result; and further comprising generating a control signal based on the previous logical state for controlling whether the first result drives an output signal.

3. The method of claim 2, wherein generating the control signal includes comparing the oscillating reference and the output signal.

4. (Once Amended) The method of claim 3, wherein the first result drives the output signal from the previous logical state toward the first result; and generating a control signal includes comparing the oscillating reference and the output signal while the output signal is still logically equal to the previous logical state.

5. The method of claim 3, wherein the first result drives the output signal from the previous logical state toward the first result; and generating a control signal includes comparing the oscillating reference and the output signal after the output signal logically equals the first result.

** 6. (Once Amended) The method of claim 1, wherein the oscillating reference is received substantially synchronously with the incoming signal.

7. The method of claim 1, wherein the oscillating reference provides voltage and timing attributes.

8. The method of claim 1, wherein the oscillating reference is negated.

9. (Once Amended) The method of claim 1, further comprising:

obtaining an oscillating reference complement; and comparing the complement against the incoming signal and against the previous logical state to detect a transition in the incoming signal relative to the previous logical state.

10. The method of claim 1, wherein the oscillating reference includes an oscillating source synchronous voltage and timing reference having a slew rate and a cycle time, the slew rate being substantially equal to one-half the cycle time.

11. A system for detecting a transition in an incoming signal from a known previous logical state, comprising:

first and second input terminals for receiving, respectively, an oscillating reference and an incoming signal;

an output terminal providing an output signal logically equal to the previous logical state;

a first comparator coupled to the first and second input terminals for comparing the reference and the incoming signal to generate a first result; and

a first controller coupled to the first comparator for coupling the first result to the output terminal based on the previous logical state.

12. The system of claim 11, wherein the first controller compares the oscillating reference and the output signal.

13. The system of claim 12, wherein the first result is coupled to the output terminal to drive the output signal from the previous logical state toward the first result; and the first controller is coupled to compare

the oscillating reference and the output signal while the output signal is still logically equal to the previous logical state.

14. (Once Amended) The system of claim 12, wherein the first result is coupled to the output terminal to drive the output signal from the previous logical state toward the first result; and the first controller is coupled to compare the oscillating reference and the output signal after the output signal logically equals the first result.

** 15. (Once Amended) The method of claim 11, wherein the oscillating reference is received substantially synchronously with the incoming signal.

16. The system of claim 11, wherein the oscillating reference provides voltage and timing attributes.

17. The system of claim 11, wherein the oscillating reference is negated.

18. The system of claim 11, wherein the oscillating reference includes an oscillating source synchronous voltage and timing reference having a slew rate and a cycle time, the slew rate being substantially equal to one-half the cycle time.

19. (Once Amended) The system of claim 11, further comprising:

a third input terminal for receiving an oscillating reference complement;

a second comparator coupled to the second and third input terminals for comparing the complement and the incoming signal to generate a second result; and

a second controller coupled to the second comparator for coupling the second comparator to the output terminal based on the previous logical state.

20. (Once Amended) A method of comparing an incoming signal to a previous logical state, comprising the steps of:

obtaining an oscillating reference and an oscillating reference complement, the oscillating reference complement being a complement of the oscillating reference;

receiving the incoming signal;

comparing by a first comparator the oscillating reference against the incoming signal to generate a first result;

comparing by a second comparator the oscillating reference complement against the incoming signal to generate a second result;

using a control signal based on the previous logical state to control whether the first result or the second result passes as an output signal.

21. The method of claim 20, wherein the previous logical state previously drove the output signal via the first comparator; the incoming signal is logically the same as the previous logical state; and the control signal allows the second result to pass as the output signal.

22. (Once Amended) The method of claim 20, wherein the previous logical state previously drove the output signal via the first comparator; the incoming signal is logically opposite the previous logical state; and the control signal allows the first result to pass as the output signal.

** 23. (Twice Amended) A receiver comprising:

a first comparator for comparing an oscillating reference and a new signal;

a second comparator for comparing a complement of the oscillating reference and the new signal;

an output terminal coupled to one of the first and second comparators;

circuitry for maintaining the comparator that is coupled to the output terminal ~~coupled to the output terminal~~ when the new signal transitions; and

circuitry for coupling to the output terminal the comparator that is not coupled to the output terminal ~~the other comparator to the output terminal~~ and de-coupling ~~the coupled comparator~~ from the output terminal the comparator that is coupled to the output terminal when the new signal does not transition.

24. The method of claim 1, wherein the known previous logical state is a full-rail voltage; and the oscillating reference and incoming signal are both small-swing signals.

25. (Amended) The method of claim 24, wherein the small-swing signals swing approximately 0.5 volts.

26. The system of claim 11, wherein the known previous logical state is a full-rail voltage; and the oscillating reference and incoming signal are both small-swing signals.

27. (Amended) The system of claim 26, wherein the small-swing signals swing approximately 0.5 volts.

Please add the following *NEW* claims 28 through 33.

28. (New) The system of claim 1, wherein the oscillating reference comprises a ramp signal.

29. (New) The system of claim 1, wherein the oscillating reference is a discontinuously varying signal.

30. (New) The method of claim 11, wherein the oscillating reference comprises a ramp signal.

31. (New) The method of claim 11, wherein the oscillating reference is a discontinuously varying signal.

32. (New) The method of claim 11, wherein the first controller includes an exclusive-OR (XOR) logic gate.

33. (New) The method of claim 19, wherein the second controller includes an exclusive-OR (XOR) logic gate.